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(14) (non-volatile) and (bank block array) and (RDRAM rambus) and (clock  
 (4) (non-volatile) and (bank block array) and (RDRAM rambus) and (clock n  
 (2) ("6310814" "5511024").pn.  
 (2) ("6310814" "5511024").pn.) and (rising falling edge rambus burst non  
 (2) (non-volatile) and (bank block array) and (RDRAM rambus) and (clock n  
 (0) ("6310814" "5511024").pn.) and (rising falling edge rambus burst no  
 (2) (non volatile) and (bank block array) and (KCRAM rambus) and (clock  
 (21) (bank block array) and (clock near5 ((rising falling) near3 edge)) a  
 (10) ((bank block array) and (clock near5 ((rising falling) near3 edge)))  
 (20) ((bank block array) and (clock near5 ((rising falling) near3 edge)))  
 (43) (non-volatile nonvolatile flash) and (bank block array) and (RDRAM r  
 (18) (non-volatile nonvolatile flash) and (bank block array) and (RDRAM r  
 (18) (non-volatile nonvolatile flash) and (RDRAM rambus) and (((rising fa  
 (15) (non-volatile nonvolatile flash) and (RDRAM rambus) and (((rising an  
 (604) (output near3 (data information)) with ((risS3 with fallS3) near3 o  
 (749) (output near3 (data information)) with ((risS3 and fallS3) near3 ed  
 (14) (non-volatile nonvolatile flash) and (RDRAM rambus) and ((risS3 with  
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#	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrievable	C	Inventor	S	C	W			
1	<input type="checkbox"/> US 20020147889 20021010	21	Cache coherent protocol in which exclusive and modified	711/144					Kruckemyer, David A. et al.	<input checked="" type="checkbox"/>					
2	<input type="checkbox"/> US 20010047450 20011129	30	HIGH BANDWIDTH MEMORY INTERFACE	711/105	710/305;	711/167;			GILLINGHAM, PETER et al.	<input checked="" type="checkbox"/>					
3	<input type="checkbox"/> US 20020041633 20020411	16	Bus precharge during a phase of a clock signal to	375/259					Cho, James Y. et al.	<input checked="" type="checkbox"/>					
4	<input type="checkbox"/> US 20020174252 20021121	23	System on a chip for packet processing	709/250	709/253				Hayter, Mark D. et al.	<input checked="" type="checkbox"/>					
5	<input type="checkbox"/> US 6480946 B1 20021112	68	Memory system for synchronized and high speed	711/167	711/170;	713/400;			Tomishima, Shigeki et al.	<input checked="" type="checkbox"/>					
6	<input type="checkbox"/> US 20010044891 20011122	36	Establishing an operating mode in a processor	712/229					McGrath, Kevin J. et al.	<input checked="" type="checkbox"/>					
7	<input type="checkbox"/> US 6411152 B1 20020625	9	Conditional clock buffer circuit	327/291	327/108				Dobberpuhl, Daniel W.	<input checked="" type="checkbox"/>					
8	<input type="checkbox"/> US 6324602 B1 20011127	22	Advanced input/output interface for an integrated	710/68	341/56;	375/287;			Chen, Jawji et al.	<input checked="" type="checkbox"/>					
9	<input type="checkbox"/> US 6487648 B1 20021126	20	SDRAM controller implemented in a PLD	711/167	326/39;	713/400;			Hammoun, Joseph H.	<input checked="" type="checkbox"/>					
10	<input type="checkbox"/> US 6215696 B1 20010410	44	Memory system with switching for data isolation	365/52	361/729;	365/63;			Deneroff, Martin M. et al.	<input checked="" type="checkbox"/>					
11	<input type="checkbox"/> US 6226755 B1 20010501	11	Apparatus and method for	713/400	713/600				Reeves, Earl C.	<input checked="" type="checkbox"/>					

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